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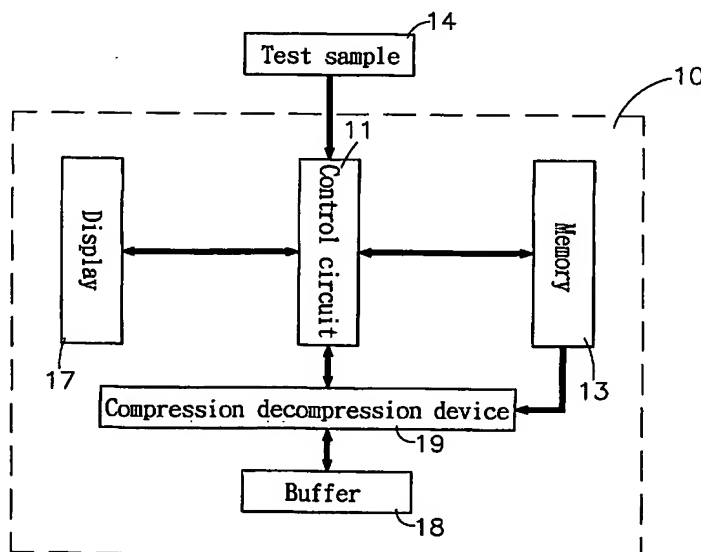
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(54) Title: PROGRAMMABLE LOGIC ANALYZER DATA ANALYZING METHOD



(57) Abstract: A programmable logic analyzer data analyzing method includes the step of controlling a control circuit (11) to fetch waveform data from the test sample (14) and to store fetched waveform data in a memory (13), the step of controlling the control circuit (11) to transmit the waveform data from the memory (13) to a computer through a transmission interface (19) when the memory space of the memory (13) is used up (fully occupied), the step of driving the computer to write the received waveform data in a buffer (18) thereof, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to use the display screen (17) of the computer for making debugging data analysis, comparison data analysis and search data analysis, to store the analyzed data in the form of a file, or to print out the analyzed data through a printer.

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**PROGRAMMABLE LOGIC ANALYZER DATA ANALYZING**  
**METHOD**

**BACKGROUND OF THE INVENTION**

**1. Field of the Invention:**

5           The present invention relates to logic analyzers and, more specifically, to a programmable logic analyzer data analyzing method, which enables the waveform data of the test sample to be fetched by a logic analyzer and then transmitted to the display screen of a computer for display, so that the user can use the  
10 displayed data to make debugging data analysis, comparison data analysis and search data analysis, to store the analyzed data in the form of a file, or to print out the analyzed data through a printer.

**2. Description of the Related Art:**

          A regular logic analyzer can simply fetch data from the test  
15 digital circuit (for example, an integrated circuit) for display on a display screen, and for further visual analysis by a man. When designing a logic analyzer, the designer may consider the factors of (1) depth of memory, (2) speed of data fetching, (3) capability of triggering, and (4) stability (anti-noise capability). According to  
20 conventional techniques, it is difficult to achieve a breakthrough. Following fast development of high technology, the limited functions of conventional logic analyzers cannot meet the requirements of programming engineers. Programming engineers

require high performance analyzer to help developing advanced products. Current logic analyzer can simply test specific items but not all products of same category. For example, a logic analyzer for testing a USB communication interface cannot be used to test other  
5 communication interface such as RS0232. Due to this drawback, a programming engineer may have to prepare various logic analyzers for different test purposes.

Therefore, it is desirable to provide a programmable logic analyzer data analyzing method that provides a complete series of  
10 functions including testing, debugging, and analyzing functions.

#### **SUMMARY OF THE INVENTION**

The present invention has been accomplished under the circumstances in view. According to one embodiment of the present invention, the programmable logic analyzer data analyzing method  
15 comprises the step of controlling a control circuit to fetch waveform data from the test sample and to store fetched waveform data in a memory, the step of controlling the control circuit to transmit the waveform data from the memory to a computer through a transmission interface when the memory space of the memory  
20 used up (fully occupied), the step of driving the computer to write the received waveform data in a buffer thereof, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to use the displayed on the display screen of the

computer for making debugging data analysis, comparison data analysis and search data analysis, to store the analyzed data in the form of a file, or to print out the analyzed data through a printer.

According to another embodiment of the present invention, the

5 programmable logic analyzer data analyzing method comprises the step of controlling a control circuit to fetch waveform data from the test sample and to store fetched waveform data in a memory, the step of writing the waveform data in a buffer when the memory space of the memory used up (fully occupied), the step of driving  
10 the control circuit to transmit the waveform data from the buffer to a display, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to make data analyses based on the data received from the memory by the computer and displayed on a display screen of the computer.

## 15 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a circuit block diagram of a logic analyzer according to the present invention.

FIG. 1B is a circuit block diagram of an alternate form of the logic analyzer according to the present invention.

20 FIG. 2 is a flow chart of the present invention.

FIG. 3 is a flow chart of the test sample waveform quality analysis according to the present invention.

FIG. 3A is a flow chart of the output logic analysis of the

waveform quality analysis according to the present invention.

FIG. 3B is a flow chart of the waveform bandwidth analysis of the waveform quality analysis according to the present invention.

5        FIG. 3C is a flow chart of the comparison data analysis of the waveform quality analysis according to the present invention.

FIG. 3D is a flow chart of the input forbidding analysis of the waveform quality analysis according to the present invention.

10       FIG. 3E is a flow chart of the search data analysis of the waveform quality analysis according to the present invention.

FIG. 4 is a flow chart of the communication protocol analysis according to the present invention.

15       FIG. 4A is a flow chart of the debugging data analysis of the communication protocol analysis according to the present invention.

FIG. 4B is a flow chart of the search data analysis of the communication protocol analysis according to the present invention.

20       FIG. 5 is a flow chart of the memory data analysis according to the present invention.

FIG. 5A is a flow chart of the read write data analysis of the memory data analysis according to the present invention.

FIG. 5B is a flow chart of the comparison data analysis of

the memory data analysis according to the present invention.

FIG. 5C is a flow chart of the search data analysis of the memory data analysis according to the present invention.

FIG. 6A is a circuit block diagram of another alternate form  
5 of the logic analyzer according to the present invention.

FIG. 6B is a circuit block diagram of still another alternate form of the present invention.

FIG. 7 is a schematic drawing showing the display of the communication protocol display window according to the present  
10 invention.

FIG. 8 is a schematic drawing showing the display of the memory data display window according to the present invention.

FIG. 9 is a schematic drawing showing the display of the logic analyzer control display window according to the present  
15 invention.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

Referring to FIG. 1A, a logic analyzer 10 in accordance with the present invention comprises a control circuit 11, a transmission interface 12, a memory 13, and a compressor 16. The  
20 control circuit 11 is connected to the test sample 14 through an implement (not shown). The transmission interface 12 is connected to a host computer 15. The control circuit 11 reads in test data from the test sample 14, and then sends obtained test data to the



compressor 16 for compression, for enabling compressed data to be further stored in the memory 13. When the memory space of the memory 13 used up (fully occupied by storage data), the control circuit 11 transmits compressed storage data from the memory 13 to  
5 the computer 15 through the transmission interface 12 for decompression by the computer 15 and for display on the display screen of the computer 15 after decompression.

FIG. 1B shows an alternate form of the logic analyzer 10. According to this alternate form, the control circuit 11 obtains test  
10 data from the test sample 14, and then directly stores obtained test data in the memory 13. When the memory space of the memory 13 used up (fully occupied by storage data), the control circuit 11 retrieves storage test data from the memory 13 and sends retrieved storage test data to the compressor 16 for compression, and then  
15 drives the transmission interface 12 to transmit compressed test data from the compressor 16 to the computer 15 for decompression by the computer 15 and for display on the display screen of the computer 15 after decompression.

With reference to FIGS. 1A and 1B again, when the logic  
20 analyzer 10 received a test sample data sheet inputted by the user or when the user selected the code number of the test sample from the database, the control circuit 11 of the logic analyzer 10 fetches waveform data from the test sample 14, and then stores fetched

waveform data in the memory 13, and then drives the transmission interface 12 to transmit storage waveform data from the memory 13 to the computer 15 when the memory space of the memory 13 used up (fully occupied by storage data). Upon receipt of waveform data  
5 from the data analyzer 10, the computer 15 fills the data in a buffer, and then transmits the data from the buffer to the display screen for display. Thereafter, a test sample (digital circuit) test signal auxiliary analyzing procedure 100 is performed. This test sample test signal auxiliary analyzing procedure 100 includes waveform  
10 quality analysis 20, communication protocol analysis 30, and memory data analysis 40. Thus, the user can use the data displayed on the display screen of the computer 15 to run debugging data analysis, comparison data analysis and search data analysis, or store analyzed data in the form of a file or print out analyzed data  
15 through a printer.

Referring to FIG. 3 and FIG. 2 again, the waveform quality analysis 20 of the test sample test signal auxiliary analyzing procedure 100 works subject to the steps bellows:

- (200) Input test signal;
- 20 (201) Make a logic comparison with the data base to see if the inputted test signal meets feature specification;
- (202) Output logic analysis; at this time, proceed to step (202A) to determine if output waveform logic fits the specification or

not? And then terminate the analysis action if positive (see FIG. 3A), or proceed to step (202B) to mark the waveform display zone with another color and then terminate the analysis action if negative (see FIG. 3A and also FIG. 9);

5 (203) Waveform bandwidth analysis; at this time, proceed to step (203A) to determine if the waveform bandwidth fits the specification or not? And then terminate the analysis action if positive (see FIG. 3B), or proceed to step (203B) to mark the waveform display zone with another color and then terminate  
10 the analysis action if negative (see FIG. 3B and also FIG. 9);

(204) Comparison data analysis; at this time, proceed to step (204A) to input test signal again, and then to step (204B) to let the user select the data for comparison, and then to step (204C) to mark the currently analyzed waveform data in the  
15 waveform display zone with another color, and then terminate the analysis action (see FIG. 3C and FIG. 9);

(205) Input forbidding analysis; at this time, proceed to step (205A) to determine if input waveform logic fits the specification or not? And then terminate the analysis action if positive, or  
20 proceed to step (205B) to mark the waveform display zone with another color if negative (see FIG. 3D and also FIG. 9);

(206) Search data analysis; at this time, proceed to step (206A) where the user selects a waveform from the waveform display

zone (see FIG. 9), the communication protocol display window (see FIG. 7) skips to the communication protocol content corresponding to the selected waveform, and the analysis action is terminated after the marking of another color (see FIG. 3E);

(207) Display analyzed waveform data on the waveform display zone (see FIG. 9);

(208) Store the waveform data in the form of a file or not? And then proceed to step (209) if positive, or terminate the analysis action if negative;

(209) Store the waveform data in the form of a file, and then terminate the analysis action.

With reference to FIGS. 2 and 4, the communication protocol analysis 30 of the test sample test signal auxiliary analyzing procedure 100 works subject to the steps bellows:

(300) Convert waveform analysis data into letters, numerals, or signs to show the communication protocol content;

(301) Make a logic comparison with the database to see if it fits the specification or not;

(302) Debugging data analysis; at this time, proceed to step (302A) to determine if the waveform bandwidth fits the specification or not? And then proceed to step (302B) if positive, or to step (302D) if negative; when entered step (302B), it converts the

data into communication protocol content, and then proceeds to step (302C) to terminate of the communication protocol contents fits the specification or not? And then terminate the analysis action if positive, or proceed to step (302D) to  
5 convert the data into error message and then terminate the analysis action if negative (see FIG. 4A);

(303) Search data analysis; at this time (see also FIG. 4B), proceed to step (303A) where the user selects a communication protocol content from the communication protocol display  
10 zone (See FIG. 7), the waveform display zone (See FIG. 9) and the memory data display window (see FIG. 8) skip to the waveform and the memory content corresponding to the selected communication protocol content, and the analysis action is terminated after the marking of another color;

15 (304) Display analyzed communication protocol content on the display zone of the communication protocol display window (See FIG. 7), and then proceed to step (305);

(305) Store the displayed communication protocol content in the form of a file or not? Proceed to step (306) if positive, or  
20 terminate the analysis action if negative;

(306) Store the communication protocol content in the form of a file, and terminate the analysis action.

With reference to FIGS. 2 and 5, the memory data analysis

40 of the test sample test signal auxiliary analyzing procedure 100 works subject to the steps bellows:

5 (400) Use the data of the communication protocol content to duplicate one copy of memory content same as the test sample;

(401) Make a logical comparison with the database to see if it fits the specification or not;

10 (402) Read write data analysis; at this time (see FIG. 5A), proceed to step (402A) to determine if same address read data and write data are identical or not? And then terminate the analysis action if positive, or proceed to step (402B) to mark the memory data display window with another color and then to terminate the analysis action if negative;

15 (403) Comparison data analysis; at this time (See FIG. 5B), proceed to step (403A) to input the communication protocol content again, and then proceed to step (403B) to let the user select which data to be compared, and then proceed to step (403C) to mark the currently analyzed memory content on the memory data display window with another color (see 20 FIG. 8), and then terminate the analysis action;

(404) Search data analysis; at this time (see FIG. 5C), proceed to step (404A) where the user selects a data, an address and a data, or an address from the memory data display window

(See FIG. 8), the communication protocol display window (see FIG. 7) skips to the communication protocol content corresponding to the selected data, selected address and data, or selected address, and the analysis action is terminated after the marking of another color;

(405) Display the analyzed memory data on the memory data display window (see FIG. 8);

(406) Store the analyzed memory data in the form of a file? And then proceed to step (407) when positive, or terminate the analysis action when negative;

(407) Store the analyzed memory data in the form of a file, and then terminate the analysis action.

FIG. 6A shows another alternate form of the logic analyzer 10. According to this design, the logic analyzer 10 is comprised of a control circuit 11, a memory 13, a display 17, and a buffer 18. The control circuit 11 is connected to the test sample 14 through an implement. During operation, the control circuit 11 reads in test data from the test sample 14, and then stores obtained test data in the memory 13. When the memory space of the memory 13 used up (fully occupied by storage data), the control circuit 11 transmits storage data from the memory 13 to the buffer 18, and then transmits the data from the buffer 18 to the display 17 for display. Further, when the logic analyzer 10 received a test sample data

sheet inputted by the user or a test sample code number selected from the database of the logic analyzer 10 by the user, the control circuit 11 fetches the waveform data from the test sample 14, and then stores the fetched data in the memory 13, and then transmits  
5 the data from the memory 13 to the buffer 18 when the memory space of the memory used up (fully occupied), and then transmits the data from the buffer 18 to the display 17 for display, and then runs the waveform quality analysis 20, communication protocol analysis 30 and memory data analysis 40 of the test sample test  
10 signal auxiliary analyzing procedure 100 (see FIG. 2). Thus, the user can use the data displayed on the display 17 for making debugging data analysis, comparison data analysis, search data analysis, etc., store the analyzed data in the form of a file, or print out the analyzed data through a printer. This logic analyzer 10  
15 further comprises a compression decompression device 19, which compresses data obtained by the control circuit 11 from the test sample 14 before storing in the memory 13, and decompresses the storage data for display on the display 17 when the memory space of the memory 13 used up (fully occupied).

20 FIG. 6B shows still another alternate form of the logic analyzer 10. According to this design, the control circuit 11 directly stores the fetched test data from the test sample 14 in the memory 13, and then drives the compression decompression device



19 to compress the storage data when the memory space of the memory 13 used up (fully occupied), and then stores the compressed data in the buffer 18, and then drives the compression decompression device 19 to decompress the compressed data, and  
5 then transmits the decompressed data to the display 17 for display.

According to the embodiments shown in FIGS. 6A and 6B, the capacity of the buffer 18 of the computer 15 or the capacity of the buffer 18 of the logic analyzer 10 varies with the amount of the internal data of the test sample 14.

10 A prototype of programmable logic analyzer data analyzing method has been constructed with the features of the annexed drawings of FIGS.1~9. The programmable logic analyzer data analyzing method functions smoothly to provide all of the features discussed earlier.

15 Although particular embodiments of the invention have been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims.

**What the invention claimed is:**

1. A programmable logic analyzer data analyzing method comprising the step of controlling a control circuit to fetch waveform data from the test sample and to store fetched waveform data in a memory, the step of controlling said control circuit to transmit the waveform data from said memory to a computer through a transmission interface when the memory space of said memory used up (fully occupied), the step of driving said computer to write the received waveform data in a buffer thereof, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to make data analyses based on the data received from said memory by said computer and displayed on a display screen of said computer.

2. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure includes a waveform quality analysis function.

3. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure includes a communication protocol analysis function.

4. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein said test sample test signal

auxiliary analyzing procedure includes a memory data analysis function.

5       5. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein when said control circuit fetched said waveform data from said test sample, a test sample data sheet inputted by the user is used for making the related analysis. .

10       6. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein when said control circuit fetched said waveform data from said test sample, the code number of the test sample selected from a database by the user is used for making the related analysis.

15       7. The programmable logic analyzer data analyzing method as claimed in claim 1 further comprising the step of storing analyzed data in the form of a file.

8. The programmable logic analyzer data analyzing method as claimed in claim 1 further comprising the step of printing out analyzed data through a printer.

20       9. The programmable logic analyzer data analyzing method as claimed in claim 1 wherein the capacity of the buffer of said computer varies with the amount of the internal data of said test sample. .

10. The programmable logic analyzer data analyzing

method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure makes a debugging data analysis on the data fetched from said test sample.

11. The programmable logic analyzer data analyzing  
5 method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure makes a comparison data analysis on the data fetched from said test sample.

12. The programmable logic analyzer data analyzing  
10 method as claimed in claim 1 wherein said test sample test signal auxiliary analyzing procedure makes a search data analysis on the data fetched from said test sample.

13. The programmable logic analyzer data analyzing  
method as claimed in claim 1 further comprising the sub-step of  
using a compressor to compress the waveform data fetched by said  
15 control circuit from said test sample before driving said control circuit to store the fetched waveform data in said memory.

14. The programmable logic analyzer data analyzing  
method as claimed in claim 1 further comprising the sub-step of  
using a compressor to compress the storage waveform data for  
20 enabling compressed waveform data to be transmitted to said computer during the step of controlling said control circuit to transmit the waveform data from said memory to a computer through a transmission interface when the memory space of said

memory used up (fully occupied).

15. A programmable logic analyzer data analyzing method comprising the step of controlling a control circuit to fetch waveform data from the test sample and to store fetched waveform data in a memory, the step of writing the waveform data in a buffer when the memory space of said memory used up (fully occupied), the step of driving said control circuit to transmit the waveform data from said buffer to a display, and the step of running a test sample test signal auxiliary analyzing procedure for enabling the user to make data analyses based on the data received from said memory by said computer and displayed on a display screen of said computer.

16. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure includes a waveform quality analysis function.

17. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure includes a communication protocol analysis function.

18. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure includes a memory data analysis

function.

19. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein when said control circuit fetched said waveform data from said test sample, a test sample data sheet inputted by the user is used for making the related analysis. .

20. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein when said control circuit fetched said waveform data from said test sample, the code number of the test sample selected from a database by the user is used for making the related analysis.

21. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the step of storing analyzed data in the form of a file.

22. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the step of printing out analyzed data through a printer.

23. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein the capacity of said buffer varies with the amount of the internal data of said test sample.

24. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure makes a debugging data analysis on

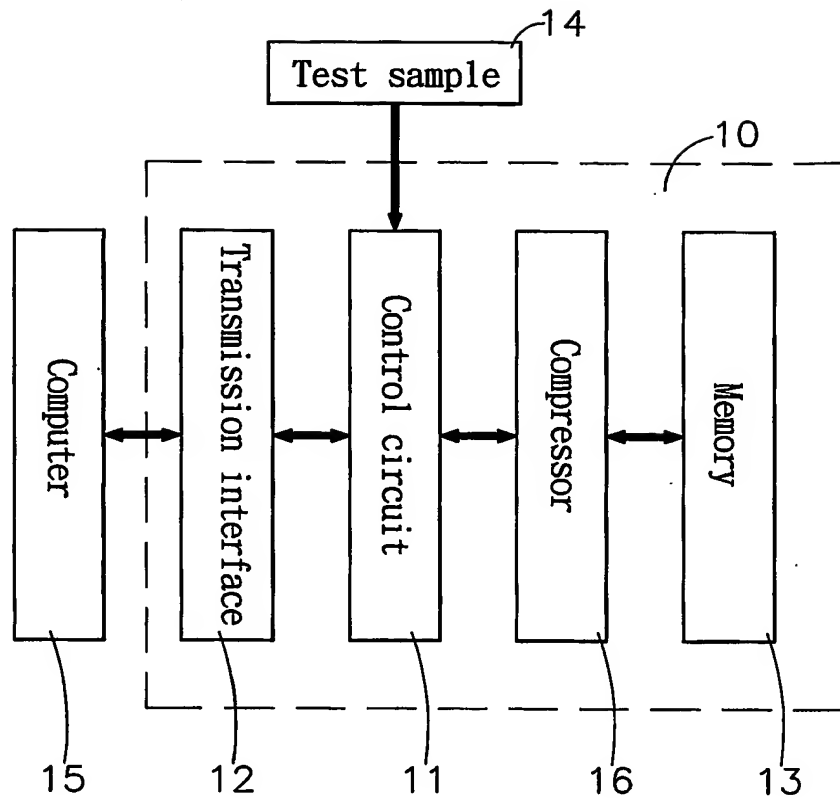
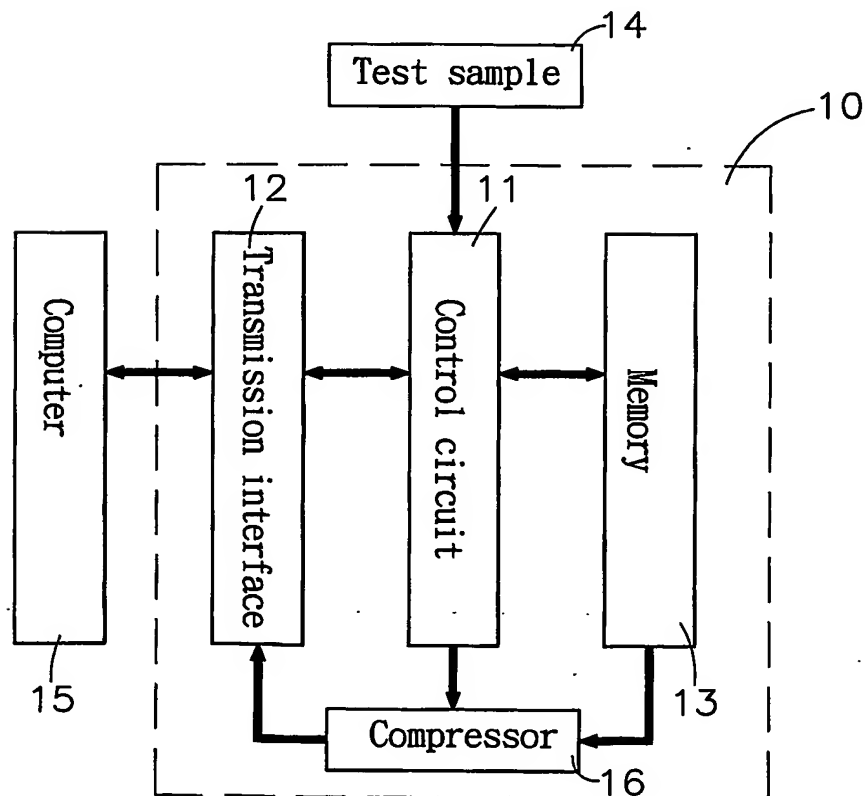
the data fetched from said test sample.

25. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure makes a comparison data analysis on  
5 the data fetched from said test sample.

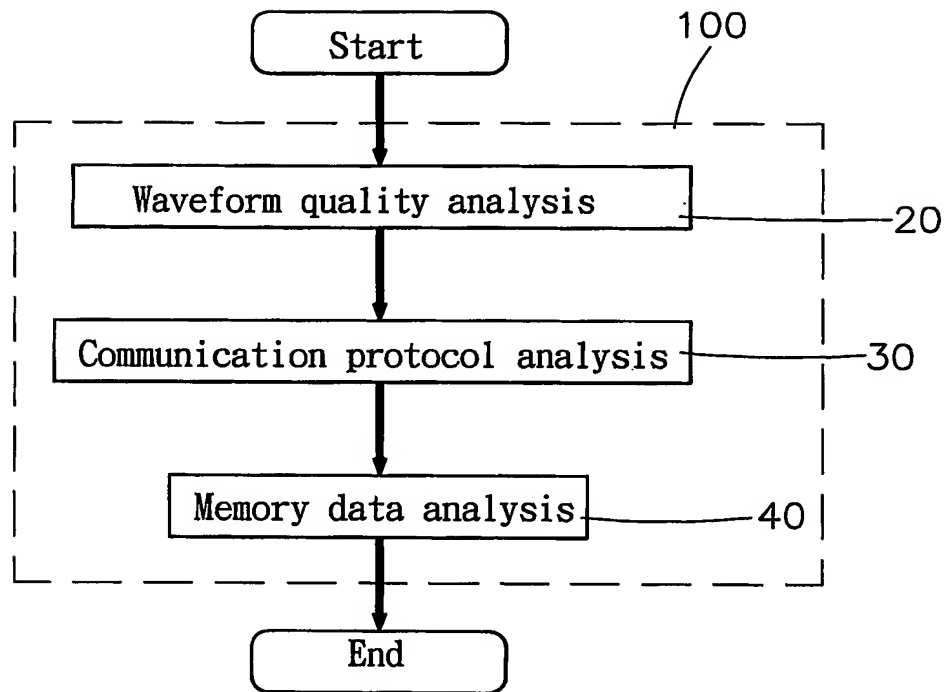
26. The programmable logic analyzer data analyzing method as claimed in claim 15 wherein said test sample test signal auxiliary analyzing procedure makes a search data analysis on the data fetched from said test sample.

10 27. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the sub-step of using a compression decompression device to compress said waveform data fetched from said test sample before storing in said memory and to decompress compressed storage waveform data  
15 before writing in said buffer after the memory capacity of said memory used up (fully occupied).

28. The programmable logic analyzer data analyzing method as claimed in claim 15 further comprising the sub-step of using a compression decompression device to compress said  
20 waveform data stored in said memory before writing in said buffer and to decompress the compressed waveform data before transmitting from said buffer to said display for display.

*FIG. 1A**FIG. 1B*



*FIG. 2*

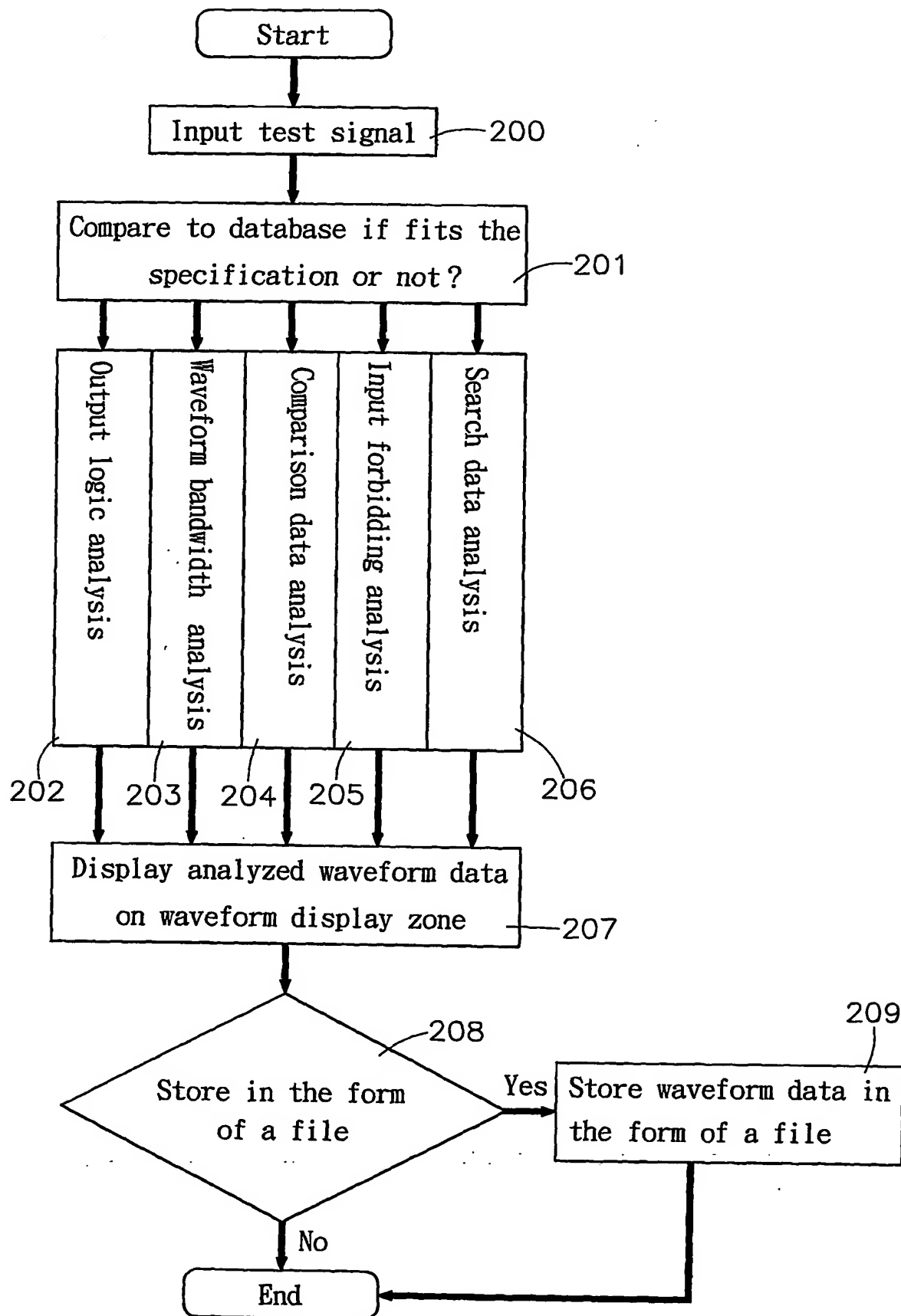
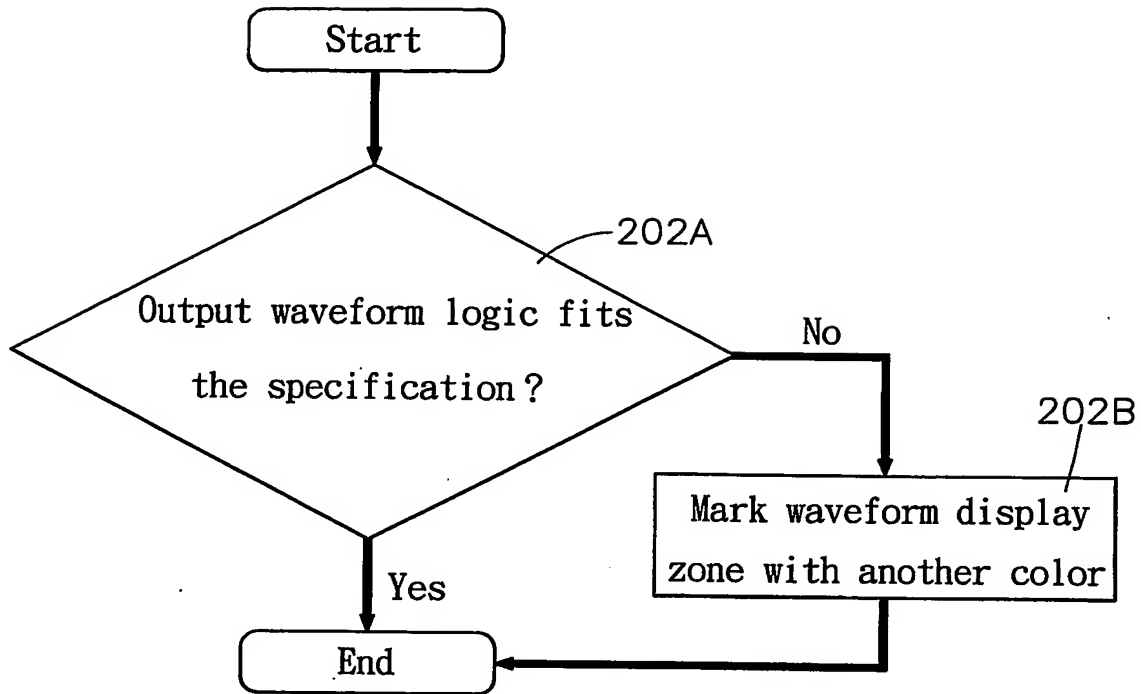
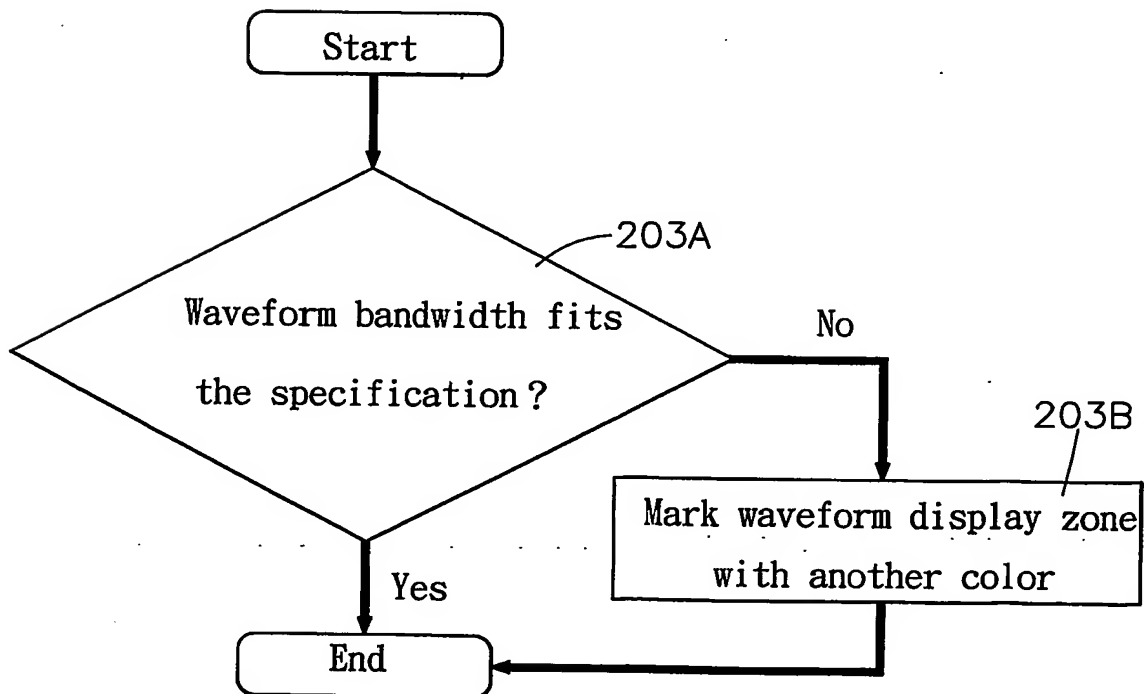
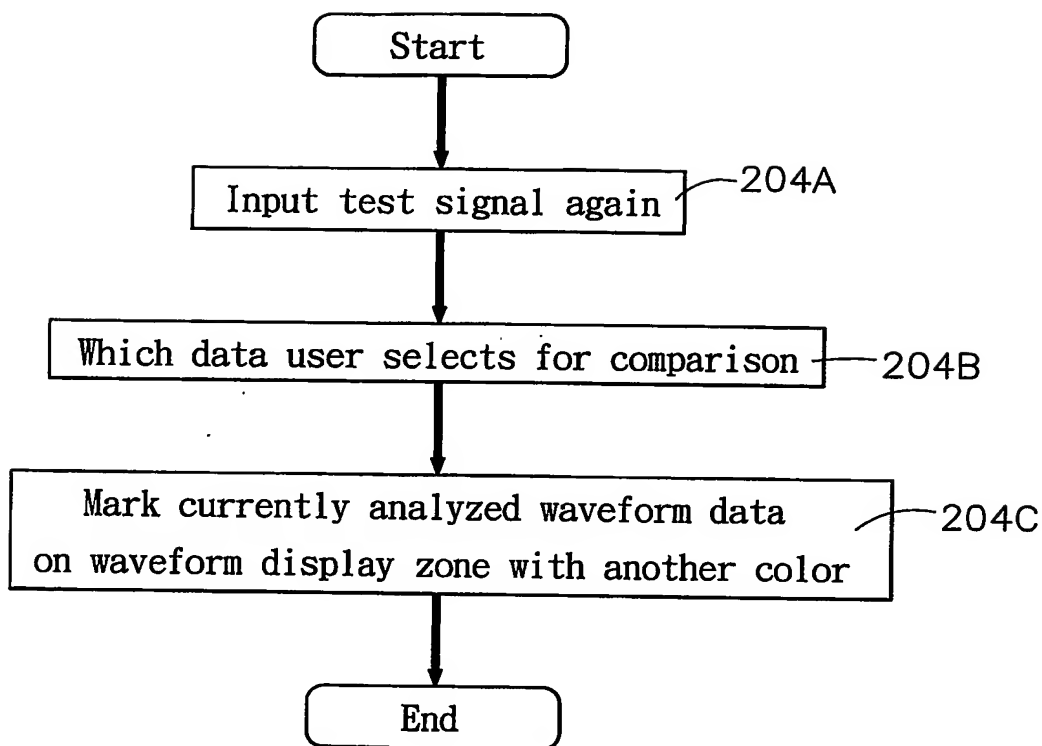
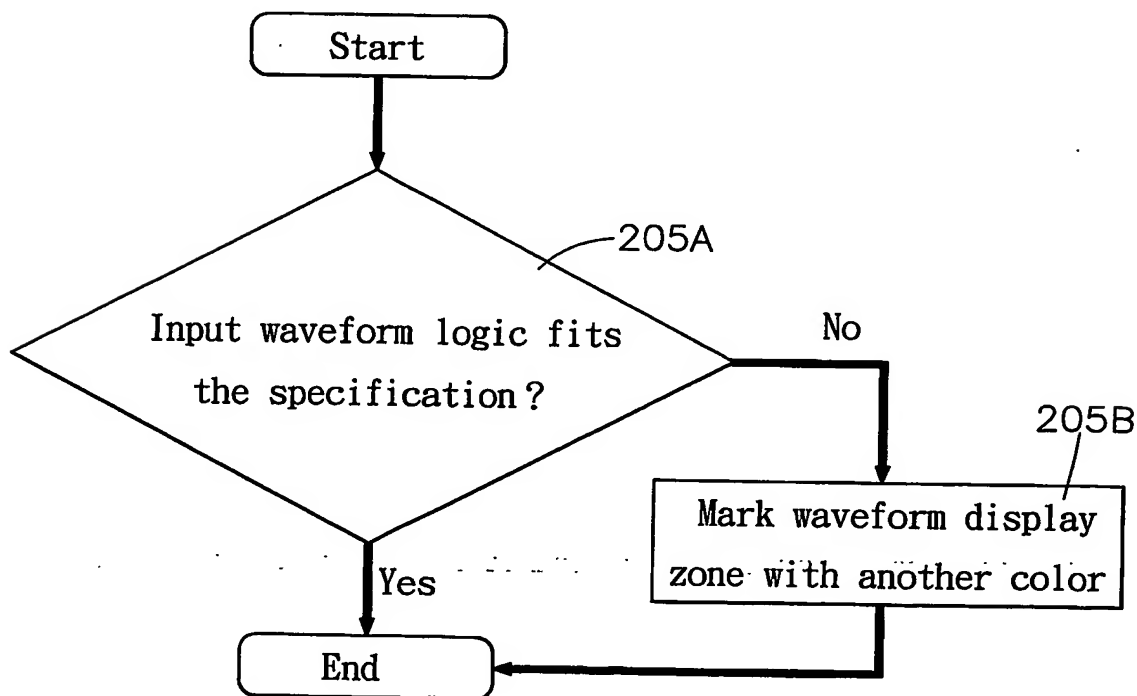
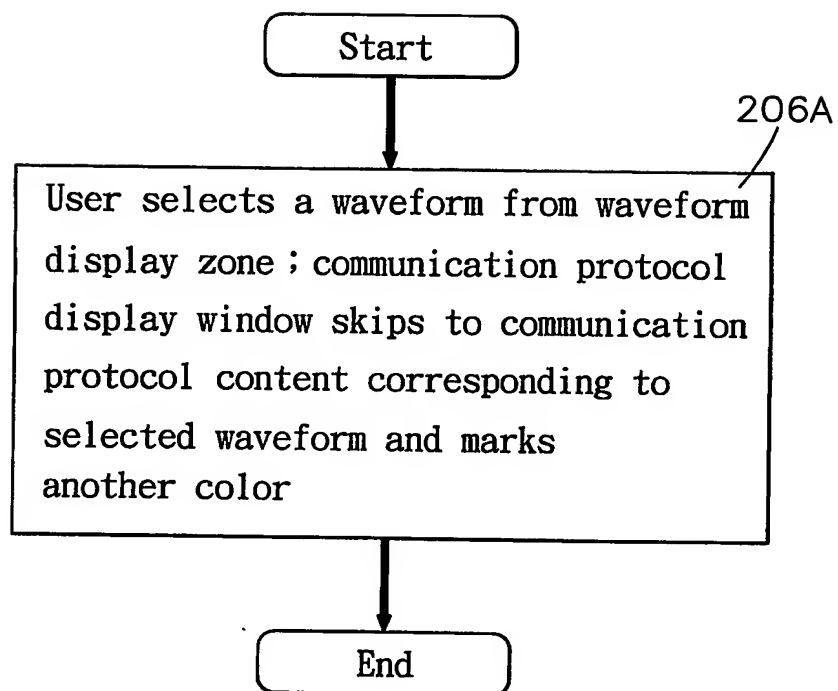


FIG. 3

*FIG. 3A**FIG. 3B*

*FIG. 3C**FIG. 3D*

*FIG. 3E*

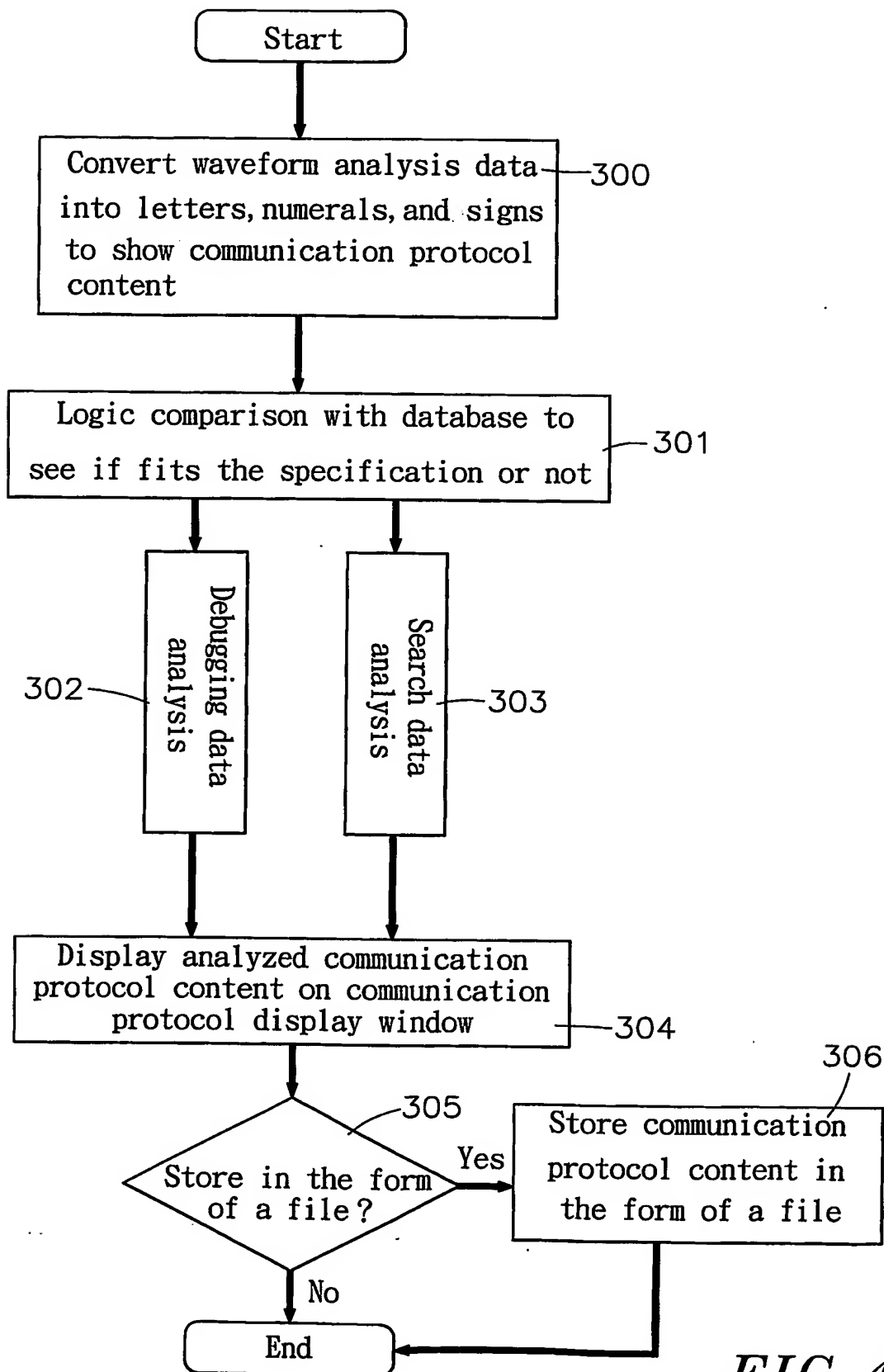
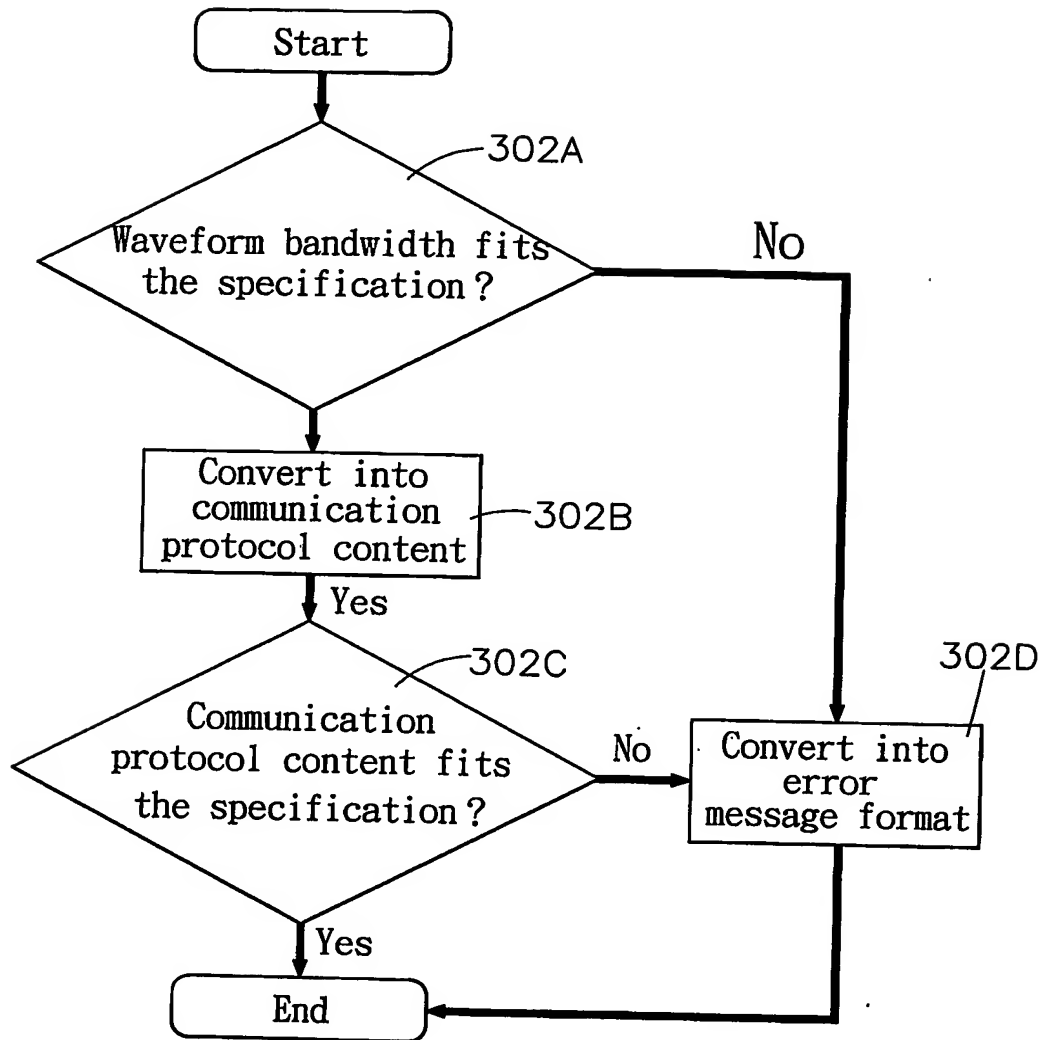
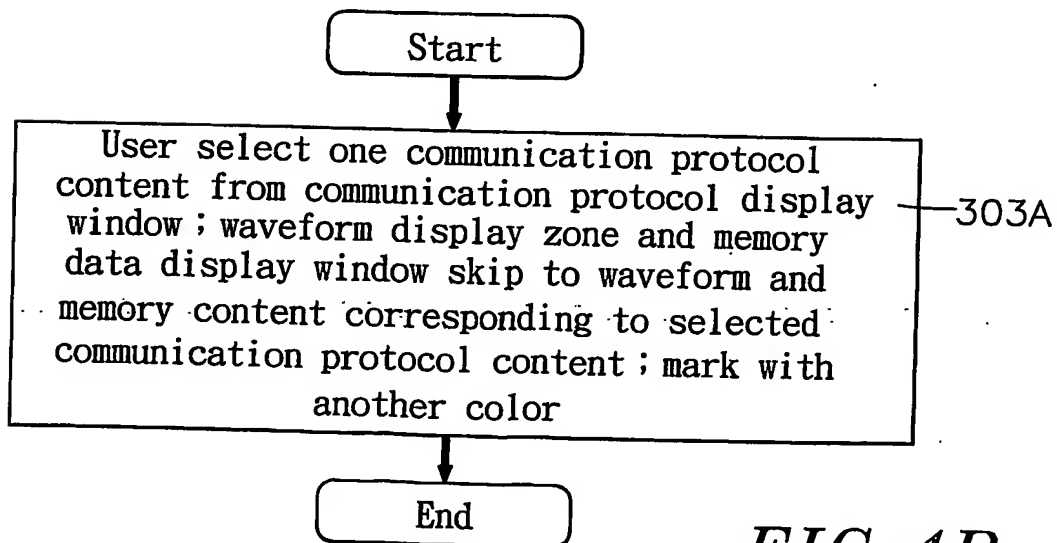
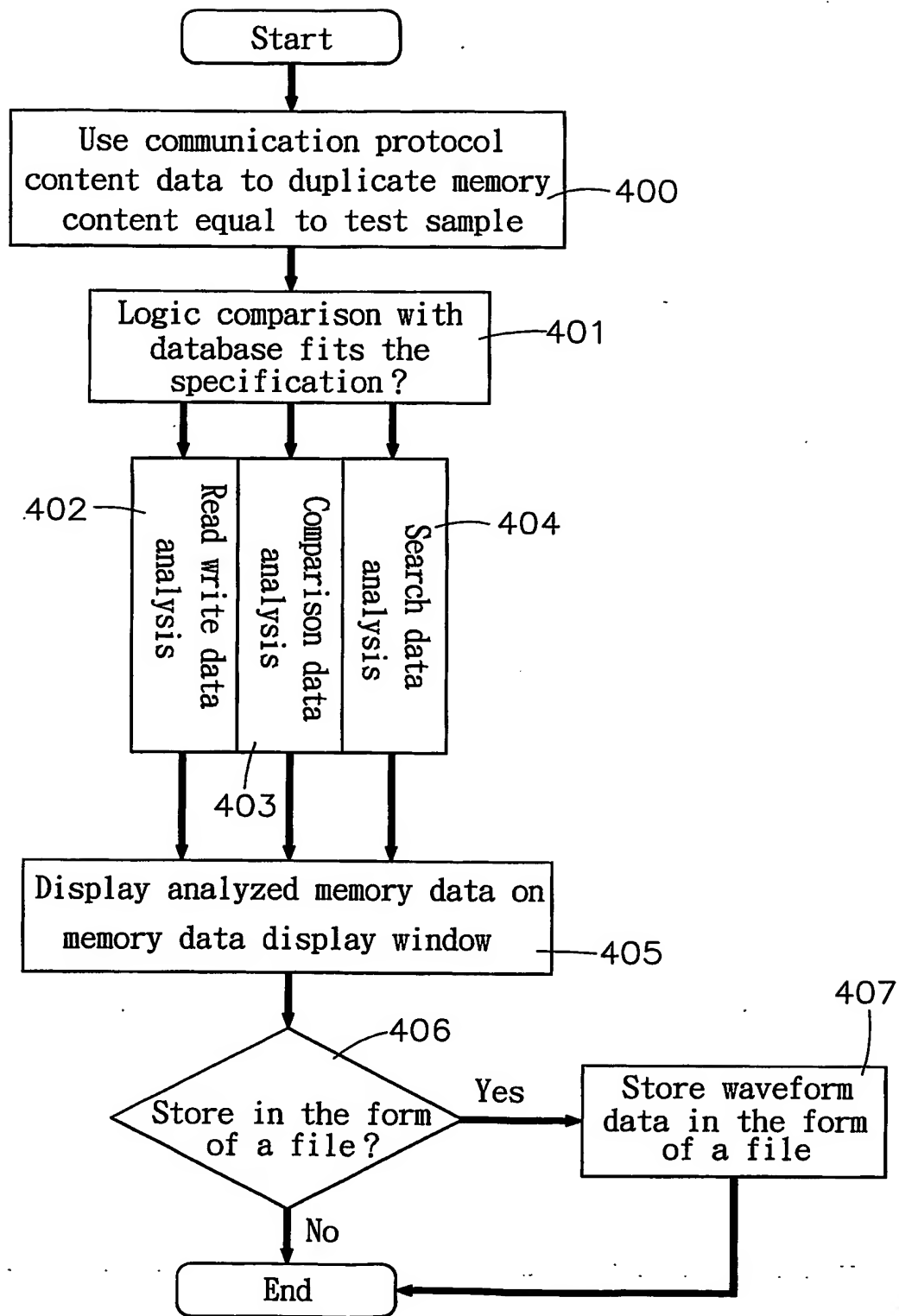
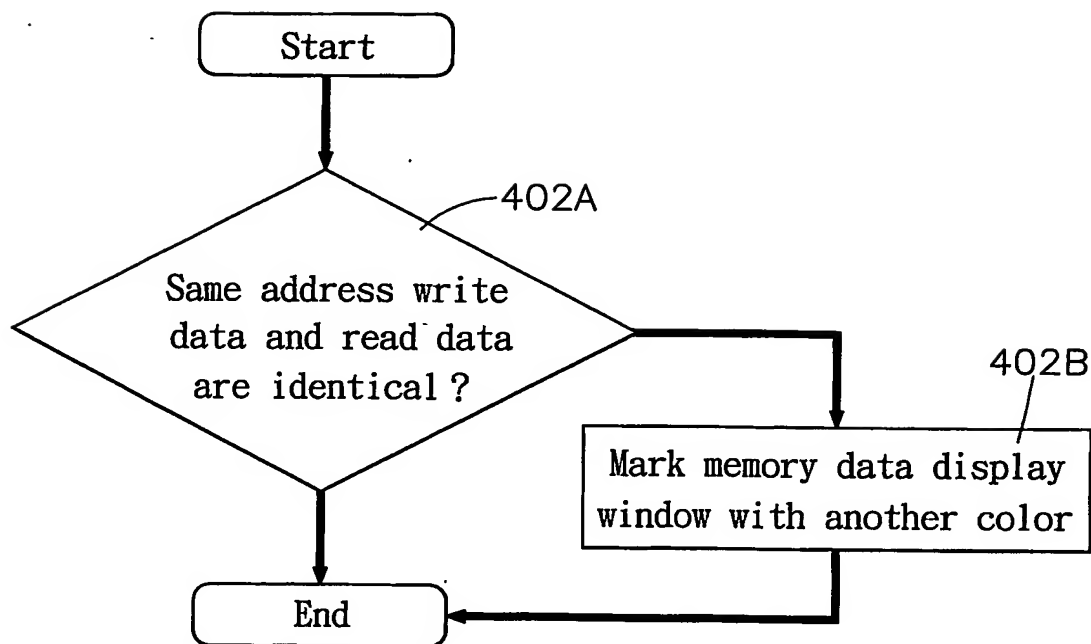
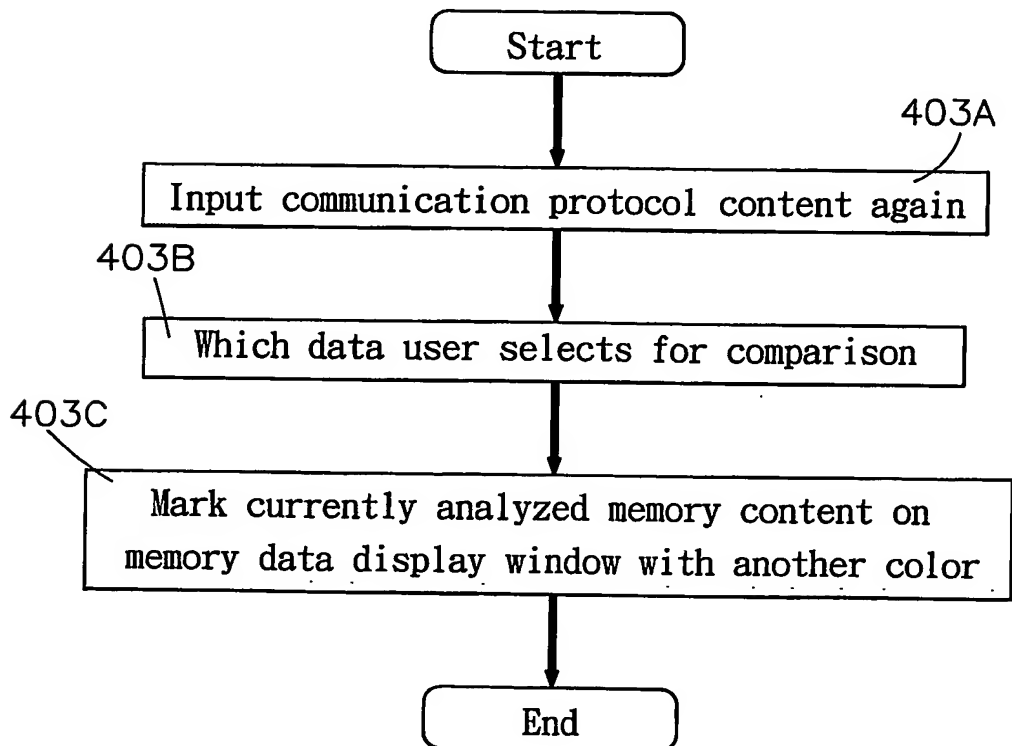


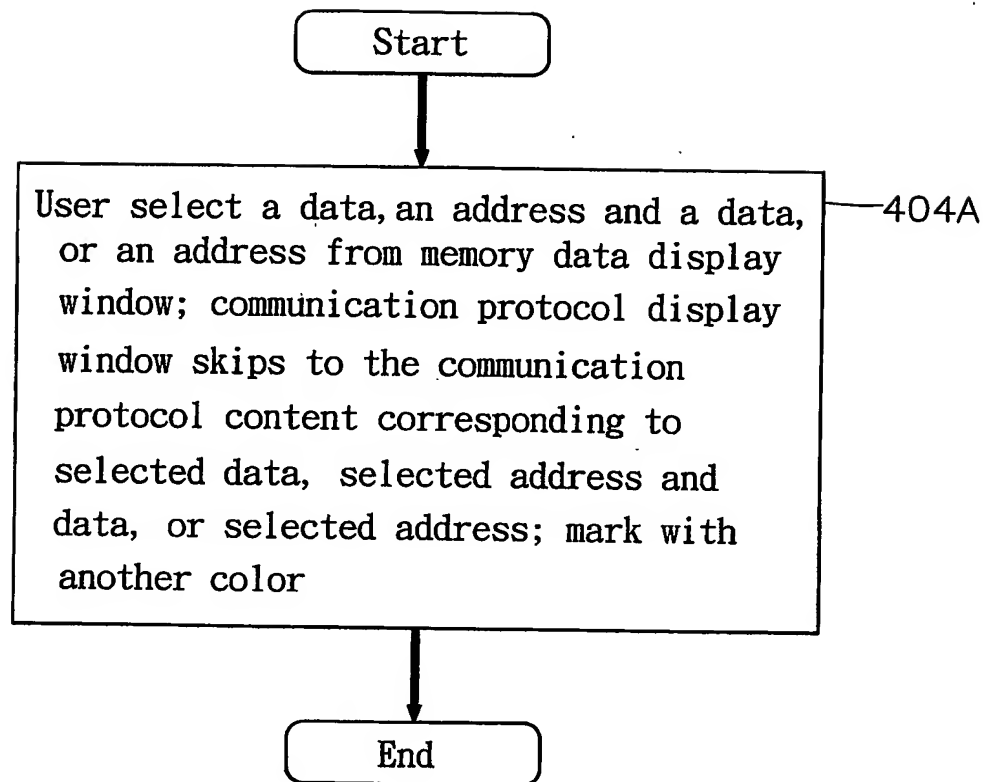
FIG. 4

*FIG. 4A**FIG. 4B*

*FIG. 5*



*FIG. 5A**FIG. 5B*

*FIG. 5C*

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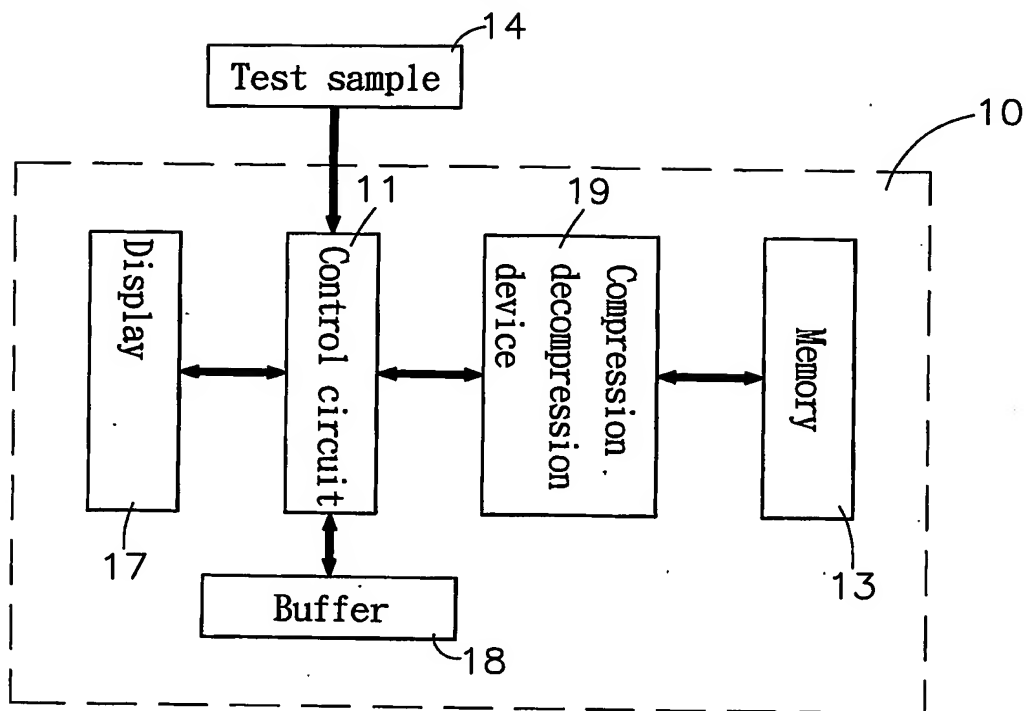


FIG. 6A

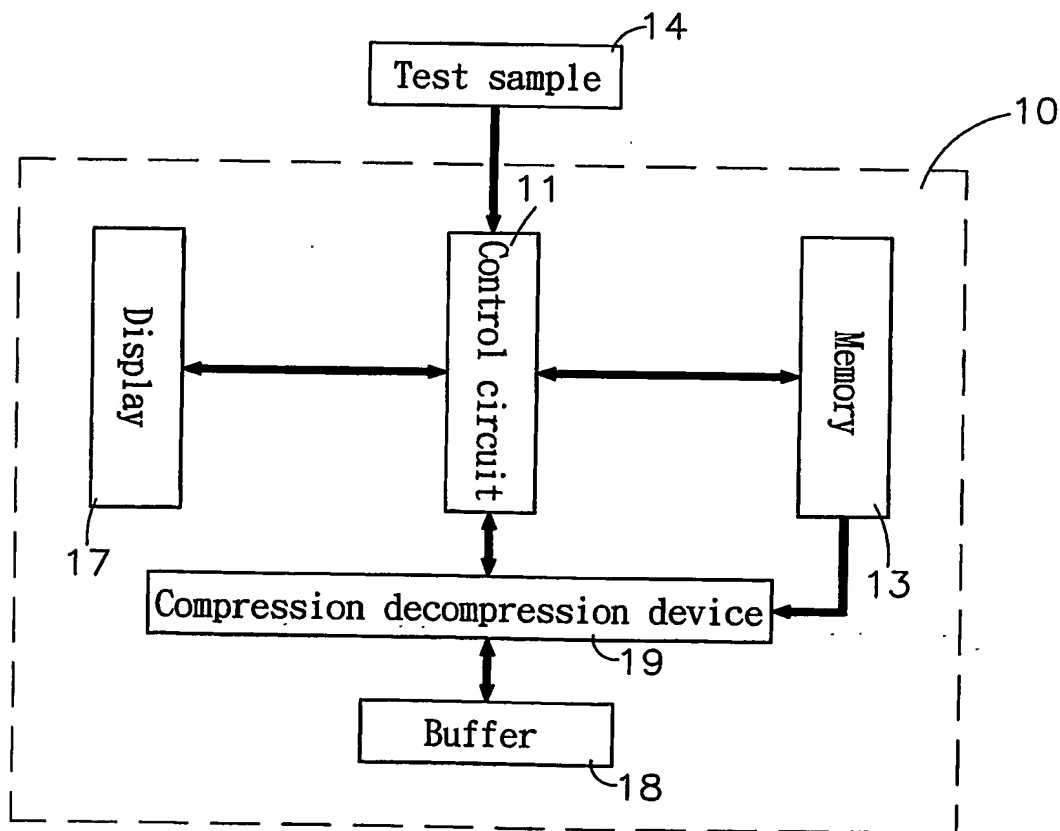


FIG. 6B

Code	Communication protocol content
0000	:
0010	
0002	
0003	
0004	
0005	
0006	
0007	
0008	
0009	
0010	

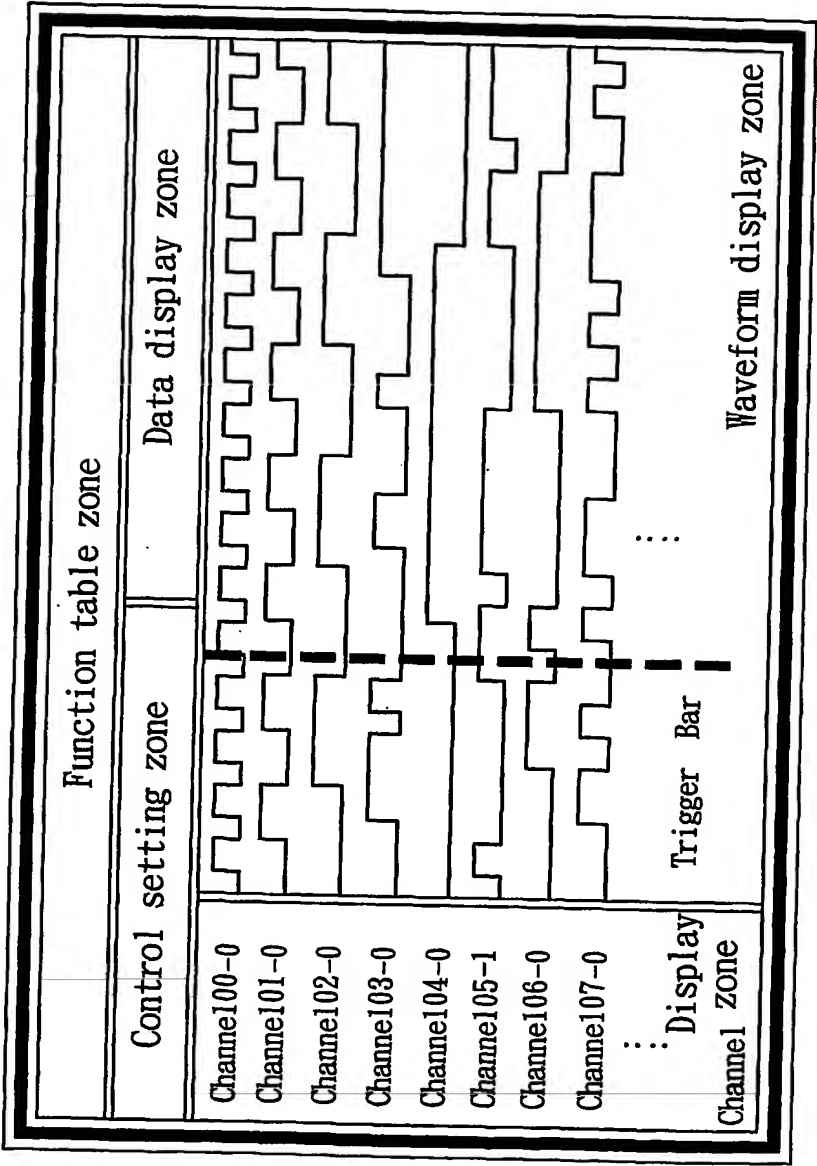
Communication protocol display window

*FIG. 7*

0000	Address display zone	0C F1 99 94 00 54 84 AE 1B C1 62 38 65 9D 71 A0
0010		00 23 47 58 57 55 23 AE 1B CC 99 A0 11 8D 71 72
0020		21 11 A0 B4 E0 F4 04 A1 CB EC D2 E8 A5 DD 7A 45
0030		33 44 99 55 00 51 8A 22 1E C2 63 38 61 90 1C AA
0040		D1 15 29 34 10 74 34 FE 11 1C 6C D8 15 1D 11 19
0050		77 25 99 94 00 84 A1 13 CC 6D E8 6D 15 1D 11 A0
0060		01 15 99 BB 00 54 84 AE 1B CC 62 38 65 9D 71 50
0070		21 11 A0 B4 E0 F4 04 A1 CB EC D2 E8 A5 DD 7A 00
.....		.....
		Data display zone

Memory data display window

*FIG. 8*



Logic analyzer control display window

FIG.9

# INTERNATIONAL SEARCH REPORT

International application No.

PCT/US02/38991

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G01R 31/28

US CL : 714/712,724

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
U.S. : 714/712,724

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
USPTO, US-PGPUB, DERWENT, IBMTDB, JPO, EPO

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4414638 A (TALAMBIRAS) 08 November 1983 (08.11.1983), column 2, lines 55-68, column 3, lines 20-31 and Figure 1.	1-28
X	US 4507740 A (STAR et al) 26 March 1985 (26.03.1985), column 2, lines 42-68, Abstract and Figure 1.	1-28
Y	US 4615027 A (RAJKAI et al) 30 September 1986 (30.09.1986), column 2, lines 36-68 and Figure 1.	1-28
X	US 6247147 B1 (BEENSTRA et al) 12 June 2001 (12.06.2001), column 5, lines 38-67, column 30, lines 1-20 and Figures 5 and 18.	1-28
X	US 4445192 A (HAAG et al) 24 April 1984 (24.04.1984), column 2, lines 35-68, Abstract and Figure 7.	1-28
Y	US 4550407 A (COUASNON et al) 29 October 1985 (29.10.1985), column 2, lines 1-68, Abstract and Figure 1.	1-28

☐ Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

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later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"

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Date of the actual completion of the international search

26 March 2003 (26.03.2003)

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